REMARKS

Claims 1-26 are pending.

Claims 20-26 are new.

Claims 1-19 are rejected.

No new matter is added.

Applicant requests reconsideration and allowance of the claims in light of the above amendments and following remarks.

Claim Amendments

Claims 1, and 14 have been amended. Claims 20-26 are new. Support for the amendments and new claims may be found in the application as filed, for example, on pages 6-12 and FIGs. 4-8. No new matter has been added.

Claim Rejections 35 U.S.C. 102(b)

Claims 1, 6, 11, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,266,273 to Conley, et al. ("Conley").

In claim 1 a transferring circuit is configured to provide the source data from the page buffer to the correction circuit and to provide amended data to the page buffer from the correction circuit. A replicating circuit is configured to copy the source data into the page buffer and to store the amended data into another page from the page buffer.

Claim 6 similarly includes a transfer circuit configured to transfer modified data of the source data to the page buffer in response to a result of comparing the first parities with the second parities.

Claim 11 similarly includes moving the modified data to the another page through the page buffer.

Claim 14 similarly includes a transfer circuit coupled to the page buffer and the error correction circuit, and configured to transfer amended data from the error correction circuit to the page buffer.

Thus, in claims 1, 6, 11, and 14, amended data from the correction circuit passes back to the page buffer before being stored in another page from the page buffer.

The Examiner argues that Conley explicitly or implicitly teaches all claimed limitations. However, Conley does not teach the circuitry forming the path for the data as recited in claim 1, and similarly in claims 6, 11, and 14. In Conley, the data to be rewritten passes to the data register. *Conley, col. 5, ll. 20-27.* "The transfer operation occurs without modifying the original sense data register contents." *Conley, col. 6, ll. 15-17.* The transfer and verification operation is performed simultaneously with the program operation. *Conley, col. 6, ll. 18-19.* Thus, in Conley, data is passed to the sense data register and is simultaneously sent to the circuit for verification without modifying the sense data register, and programmed into another data block. The circuit does not wait until any corrected data is stored in the sense data register before programming data into another block.

Furthermore, although Conley references error recovery, there is no mention of the route of the corrected data. For example, if there is an error, the error recovery mechanism is invoked. *Conley, col. 5, ll. 32-33.* No details of the error recovery mechanism are given. Validity of the data is checked or determined, but there is no description of how it is corrected. *Conley, col. 3, ll. 20-23, and col. 6, ll. 25-27.* Thus, Conley does not teach a transfer circuit that provides amended data from the correction circuit to the page buffer. As a result, Conley does not teach each and every element of claims 1, 6, 11, and 14. The Applicant requests that the Examiner withdraw the rejections of claim 1, 6, 11, and 14.

Claim Rejections 35 U.S.C. 103(a)

Claims 2-5, 7-10, 12-13, and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Conley.

The addition of the knowledge of one skilled in the art, as evidenced by U.S. Patents Nos. 4,358,848 and 4,453,251 describing error correction, does not cure the deficiencies of Conley described above. In fact, Conley suggests against transferring amended data through the data register. As described above, "The transfer operation occurs without modifying the original sense data register contents." *Conley, col. 6, ll. 15-17.* This enables the simultaneous programming and verification of Conley. *Conley, col. 6, ll. 18-19.* Thus, in the programming operation, the sense data register is not modified. As a result, Conley does not teach or suggest each and every element of claims 1-19. The applicant requests that the Examiner withdraw the rejections of claims 1-19.

Claim 26 recites that the page buffer includes only one register. As seen in FIGs. 2, 5, and 6, and described in col. 5, ll. 53-59, Conley includes two registers, a Master register and a Slave register. As described above, the two registers are needed in Conley to achieve the simultaneous programming and verification described in Conley. Thus, one skilled in the art would not modify the two registers of Conley into one register. As a result, Conley does not teach or suggest each and every element of claim 26.

Claim 23 as amended recites "a line parity circuit coupled to the page buffer and configured to generate a plurality of pairs of line parities, for each line parity pair, a first line parity associated with a first half of the lines, and a second line parity associated with a second half of the lines; and a column parity circuit coupled to the page buffer and configured to generate a plurality of pairs of column parities, for each column parity pair, a first column parity of the pair associated with a first half of the columns, and a second column parity of the pair associated with a second half of the columns."

The Examiner stated that claims 2-5, 7-10, 12-13, and 15-19 were rejected as unpatentable over Conley in that "any such ECC method in combination with that taught in Conley is considered to be obvious to one of ordinary skill in the art," as evidenced by U.S. Patents Nos. 4,358,848 to Osman and 4,453,251 to Patel. *Office Action dated April 18, 2006, p. 3.* Although the Applicant recognizes that some error code correction techniques as shown in Osman and Patel were known to one of ordinary skill in the art, circuitry for generating line parities and column parities as recited in claim 14 are not taught or suggested by Conley in light of the knowledge of one of ordinary skill in the art as evidenced by Osman and Patel.

For example, in Osman, "each parity bit in a particular row of array A_1 is generated from the data bits in that same row." *Osman, col. 3, ll. 51-52.* "Each of the parity bits in rows R_1 through R_M and columns C_1 through C_N of array A_{X+1} is generated from the data word at the corresponding row-column pair in the other arrays A_1 through A_X." *Osman, col. 4, ll. 1-4.* "Parity bits in column C_{N+1} of array A_{X+1} are generated from the parity bits in column C_{N+1} of all of the other arrays A_1 through A_X." *Osman, col. 4, ll. 11-13.* Thus, each parity bit, whether as part of an array or as a parity for rows of arrays in array A_{X+1}, does not have a corresponding parity bit forming a pair where each of the pair is associated with one half of lines or columns as recited in claim 23.

Furthermore, in Patel, an M bit word parity vector for each M byte word is generated by checking each byte for parity by generating a parity bit. *Patel, col. 1, ll. 39-44.* In a 15 byte word, the first 14 bytes are for data with the 15th byte for a dual function error correcting check character. *Patel, col. 2, ll. 60-64, and FIG. 5a.* A block parity byte is a modulo-2 sum of the value of all supplied data bytes assigned to a data block. *Patel, col. 3, ll. 4-9, and FIG. 5b.* Thus, similar to the deficiency in Osman, Patel does not teach or suggest a corresponding parity bit forming a pair where each of the pair is associated with one half of lines or columns as recited in claim 23.

As a result, Conley in view of the knowledge of one of ordinary skill in the art as evidenced by Patel and Osman does not teach or suggest each and every element of claims 23-25.

Claim 24 recites "for each column parity: an exclusive-or logic circuit configured to receive bits from the associated half of the columns and generate a result of an exclusive-or operation on bits from the associated half of the columns." Osman does not teach or suggest such circuitry for generating a result of an exclusive-or operation on bits from the associated half of the columns. Patel does describe logic blocks 41 to exclusive-or the inputs. *Patel, col. 6, ll. 26-29.* However, there is no pair of parity bits described formed form first and second halves of columns. For example, for logic circuit 41-0 having 1, 2 and 5 as inputs, there is no corresponding logic circuit 41 having 0, 3, 4, 6 and 7 as inputs. *Patel, FIG. 6.* As a result, Conley in view of the knowledge of one of ordinary skill in the art as evidenced by Patel and Osman does not teach or suggest each and every element of claims 24, and dependent claim 25.

Claim 24 recites "an exclusive-or logic circuit configured to generate a result of an exclusive-or operation on bits from a selected one of the lines; and a gate having a first input configured to receive an associated clock control signal, a second input coupled to the output of the exclusive-or logic circuit, and an output coupled to the second input of the exclusive-or gate." Although Osman describes generating a parity from the output of all exclusive-or gates of arrays A_1 through A_{Xi}, Conley in view of the knowledge of one of ordinary skill in the art as evidenced by Patel and Osman does not teach or suggest such a gate with an associated clock control signal and exclusive-or logic circuits as an inputs as recited in claims 24 and dependent claim 25. *See Osman, col. 6, ll. 20-25.*

Claim 24 recites "a plurality of unit blocks, each unit block including: an input/output line; a plurality of latches, each latch coupled to an associated bitline of the buffering and sensing logic block; and a plurality of column gates coupled to the latches and configured to selectively couple one of the latches to the input/output line in response to a column gating signal." Although Conley may describe a data register for storing a block of data and Osman describes transistors for selecting a column for a particular bit Bx, Conley in view of the knowledge of one of ordinary skill in the art as evidenced by Patel and Osman does not teach or suggest such latches and column gates as recited in claims 24 and dependent claim 25. *See Conley, col. 5, ll. 26-27, and FIG. 5, and Osman, FIG. 3.*

Claim 22 recites "a plurality of pairs of line parities, for each line parity pair, a first line parity associated with a first half of the lines, and a second line parity associated with a second half of the lines; and a plurality of pairs of column parities, for each column parity pair, a first column parity of the pair associated with a first half of the columns, and a second column parity of the pair associated with a second half of the columns." As described above, Conley in view of the knowledge of one of ordinary skill in the art as evidenced by Patel and Osman does not teach or suggest such parities associated with halves of columns or lines.

Claim 23 recites "generating a result of an exclusive-or operation on bits of the line in columns associated with the column parity." As described above, Conley in view of the knowledge of one of ordinary skill in the art as evidenced by Patel and Osman does not teach or suggest such an exclusive-or operation on bits of a line associated with a half of the columns.

Claim 24 recites "generating a result of an exclusive-or operation on bits of the line; and for each line parity associated with the line: updating the parity accumulator associated with the line parity." As described above, Conley in view of the knowledge of one of ordinary skill in the art as evidenced by Patel and Osman does not teach or suggest updating a line parity with associated exclusive-or operation results on associated lines.

Claim 25 recites "control signal generator coupled to the first inputs of the gates and the column gates, the clock control signal generator configured to generate the clock control signals associated with the gates and the column gating signals; wherein the control signal generator is configured to generate the clock control signals associated with gates associated with a line indicated by the column gating signals." As recited in claim 26, a gate is associated with each parity accumulator for each line parity. As recited in claim 25, each line parity is associated with

a corresponding half of the lines. The control signal generator is configured to generate the clock control signals associated with gates associated with a line indicated by the column gating signals. Thus, for a line indicated by the column gating signals, line parities associated with the line may be updated gated by the associated clock control signals. Conley in view of the knowledge of one of ordinary skill in the art as evidenced by Patel and Osman does not teach or suggest such a control signal generator to generate clock control signals associated with lines parities associated with a particular line as recited in claim 25.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 6, 8-11 and 13-27 of the application as amended is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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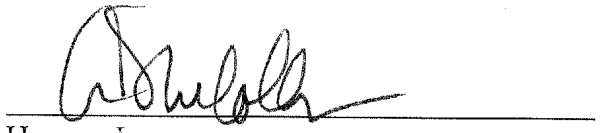

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